## <u>CLAIMS</u>

What is claimed is:

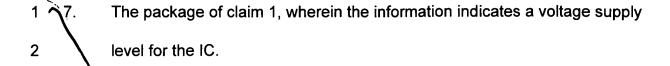
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An integrated circuit (IC) package comprising:

a substrate including an IC;

- \ a ground line; and
- an encoded region to provide information based upon selective deposition

  of solder balls electrically coupled to the ground line.
- 1 2. The package of claim 1, wherein the substrate is the substrate of a ball grid array (BGA) package.
- 1 3. The package of claim 2, wherein the IC is a processor.
- The package of claim 3, wherein a deposited solder ball in a solder ball area of the encoded region is used to denote a logical "0", and an absence of a solder ball in the solder ball area is used to denote a logical "1".
- 1 5. The package of claim 4, wherein the encoded region includes at least three solder ball areas.
- 1 6. The package of claim 5, wherein the information indicates a voltage supply
  2 level for the IC.



- 1 8. An electronic component comprising:
- a ball grid array (BGA) package including an encoded region to provide
  information based upon selective deposition of solder balls; and
  a printed circuit board (PCB) coupled to the package.
  - 9. The component of claim 8, wherein the BGA package contains a processor.
- 1 10. The package of claim 9, wherein a deposited solder ball in a solder ball area 2 of the encoded region is used to denote a logical "0", and an absence of a 3 solder ball in the solder ball area is used to denote a logical "1".
- 1 11. The package of claim 8, wherein any deposited solder ball in a solder ball
  2 area of the encoded region is electrically coupled to a first node of a resistor
  3 on the PCB, and a second node of the resistor is electrically coupled to a
  4 power trace on the PCB.
- 1 12. The package of claim 11, wherein the first node is approximately ground if a solder ball is deposited in the solder ball area, and the first node is approximately Vcc if a solder ball is absent from the solder ball area.

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|---|-----|---|
| 1 | 13. | The package of claim 12, wherein the encoded region includes at least three     |
| 2 |     | solder ball areas.  |
| 1 |     |   |
| 1 | 14. | The package of claim 13, wherein the information indicates a voltage supply     |
| 2 |     | level for a processor within the BGA package.                                   |
| 1 | 15. | A method of encoding information in an integrated circuit (IC) package, the     |
| 2 |     | method comprising:  |
| 3 |     | depositing a first solder ball in a first solder ball area of an encoded region |
| 4 |     | of an IC package to denote a first logical level; and                           |
| 5 |     | preventing a solder ball from being deposited in a second solder ball area      |
| 6 |     | of the encoded region of the IC package to denote a second logical              |
| 7 |     | level.  |
| 1 | 16. | The method of claim 15, wherein depositing the solder ball includes screen      |
| 2 |     | printing solder through a template comprising an opening adjacent to the first  |
| 3 |     | solder ball area, and preventing a solder ball from being deposited includes    |
| 4 |     | screen printing solder through a template comprising a closure adjacent to      |
| 5 |     | the second solder ball area,  |
| 1 | 17. | The method of claim 15, further comprising depositing a second solder ball in   |
| 2 |     | a third solder ball area of the encoded region of the IC package to denote the  |

first logical level.

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1 18. The method of claim 15, further comprising preventing a solder ball from
2 being deposited in a fourth solder ball area of the encoded region of the IC
3 package to denote the second logical level.